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PATENT ABSTRACTS OF JAPAN

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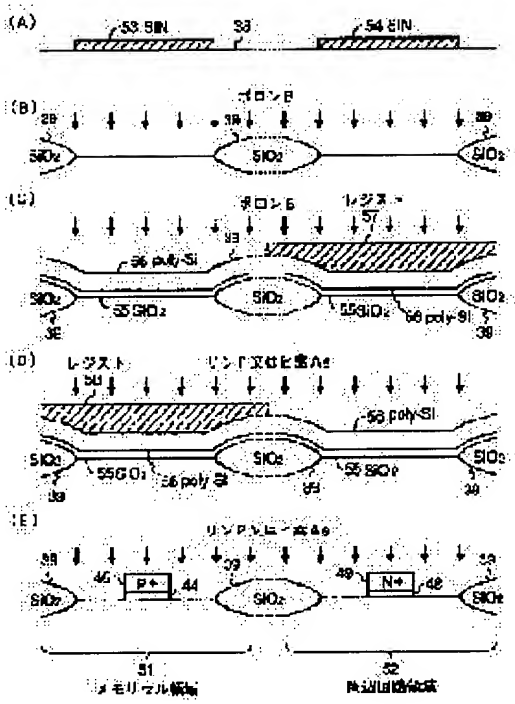
(54) DYNAMIC MEMORY

(57)Abstract:
PROBLEM TO BE SOLVED: To increase the operation voltage margin of a word line, ensure the specified value of data hold time, and cope with low voltage performance, regarding a dynamic memory wherein a dynamic cell is constituted of a capacitor and a transistor.
SOLUTION: A gate electrode 45 of an nMOS transistor 40 as a cell transistor is constituted of a P-type poly silicon layer. The amount of ion implantation of boron B for threshold voltage adjustment, which boron is implanted in a region for forming the nMOS transistor 40, is reduced. As the threshold voltage when '0' data are stored, the conventional threshold voltage is ensured, and the back bias dependence coefficient is reduced.



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to the dynamic memory which constitutes a memory cell from one capacitor and one transistor among the dynamic type semiconductor memory which uses a dynamic type memory cell for informational storage, and the so-called dynamic memory.
[0002]
[Description of the Prior Art] The word line as which drawing 4 shows the important section of an example of dynamic memory to, and WL0 and WL1 choose a memory cell, BL0 /1 are bit lines which make the data transmission line. [BL0, BL1/BL1]
[0003] Moreover, 1 and 2 are memory cells chosen by the word line WL0, and the capacitor for a charge store in 3 and 4, the so-called cell capacitor, and 5 and 6 are the transistor for a charge transfer by which ON and OFF are controlled through a word line WL0, and the so-called cell transistor.
[0004] Moreover, 7 and 8 are memory cells chosen by the word line WL1, and they are a cell capacitor and the cell transistor by which 9 and 10 mind 11, 12 mind a word line WL1, and ON and OFF are controlled.
[0005] Let the cell transistors 5, 6, 11, and 12 be nMOS transistors in this example. In addition, VCC is supply voltage.
[0006] Moreover, the line decoder which 13 decodes a line-address signal and chooses a line (word line), the sense amplifier with which 14 amplifies the difference voltage of bit lines BL0/BL0, and 15 are sense amplifiers which amplify the difference voltage of bit lines BL1/BL1.
[0007] Moreover, the train decoder which outputs the train selection signal which 16 decodes a train address signal and chooses a train, nMOS transistor to which 17 and 18 make the train selecting switch by which a flow and un-flowing are controlled by train selection-signal CL0, and 19 and 20 are nMOS transistors which make the train selecting switch by which a flow and un-flowing are controlled by train selection-signal CL1.
[0008] Moreover, the data output buffer for outputting DB/DB to a data bus, and 21 outputting data DQ outside and 22 are data input buffers which incorporate the data DQ supplied from the exterior.
[0009] Moreover, it is the rough voltage wave form chart showing the read-out operation of dynamic memory and the re-write-in operation which are shown in drawing 4 , H level (high level) is written in a memory cell 1, and when the storage node 24 of a memory cell 1 is made into supply voltage VCC, drawing 5 makes an example the case where a memory cell 1 is chosen, and is shown.
[0010] In addition, it is the pressure-up voltage which comes to carry out a pressure up in the pressure-up voltage occurrence circuit where formed VSS in the grounding voltage and VPP formed supply voltage VCC in the interior of a chip.
[0011] While it is referred to as word line WL0=VSS in front of read-out and the cell transistor 5 of a memory cell 1 is made into an OFF state here, bit lines BL0/BL0 are precharged VCC/2.
[0012] From this status, if it is word line WL0=VPP and the cell transistor 5= ON state of a memory cell 1, the storage node 24 and the bit line BL0 of a memory cell 1 will be connected through the cell transistor 5.
[0013] Consequently, the charge accumulated at the storage node 24 is outputted to a bit line BL0, and while the voltage of a bit line BL0 rises slightly from VCC/2, a sense amplifier 14 is activated after that, the difference voltage between bit lines BL [BL0/] 0 is amplified by the sense amplifier 14 and read-out is performed, re-writing to a memory cell 1 is performed.
[0014] The cell transistor which consists of a nMOS transistor here was created as conventionally shown in drawing 6 .
[0015] That is, as shown in drawing 6 A, after forming the silicon nitride 27 in the field (active region) which forms a transistor on a substrate 26 first, as the selective oxidation of the non-active region is carried out and it is shown in drawing 6 B for isolation, the field oxide film 28 is formed.
[0016] Next, in order to control the threshold voltage Vth similarly to be shown in drawing 6 B, the ion implantation of boron B which is a P type impurity is performed.
[0017] Next, as shown in drawing 6 C, the silicon oxide 29 used as a gate insulator layer is formed, and the polysilicon contest (polycrystal silicon) layer 30 used as a gate electrode is further formed on a silicon oxide 29.
[0018] Next, in order to lower resistance of a gate electrode, as the ion implantation of Lynn P which is an N type impurity, or the arsenic As is performed in the polysilicon contest layer 30, then it is shown in drawing 6 D, patterning of the gate electrode 31 is carried out.
[0019] Then, the ion implantation of Lynn P or the arsenic As is performed, and as shown in drawing 6 E, the source 33 and the

drain 34 which consist of an N type diffusion layer are formed.
[0020] Thus, the polycide which a polysilicon contest layer is used for the gate electrode of nMOS transistor which constitutes a cell transistor, or deposited the silicide compound on the upper part of a polysilicon contest layer is used.
[0021] And an N type impurity is injected into the polysilicon contest layer which makes the gate electrode of nMOS transistor which makes a cell transistor like the polysilicon contest layer which makes the gate electrode of nMOS transistor of the circumference circuit which controls a memory cell for the reduction in resistance.
[0022] Moreover, in the ion implantation process of boron B shown in drawing 6 B, it is with a cell field and a circumference circuit field, and since the suitable threshold voltages Vth differ, the amount of the ion to drive in is set as a different value, and the threshold voltage Vth of nMOS transistor which makes a cell transistor, and nMOS transistor of a circumference circuit is controlled by nMOS transistor which makes a cell transistor, and nMOS transistor of a circumference circuit to the respectively suitable value.
[0023] In order to set the voltage of VB1 and the storage node of a cell to VC1=VB1 when a cell transistor is a nMOS transistor if the voltage of the bit line in the case of writing "1" data here is set to VC1, it is necessary to carry out the voltage level VWL0 of a word line more than VB1+Vthc. However, Vthc is the threshold voltage of a cell transistor in case source potential is VB1.
[0024] Moreover, the threshold voltage Vth of an MOS transistor Since it becomes high with elevation of source potential according to the back-bias effect, The voltage of the bit line in the case of writing in "0" data is set to VB0 (usually 0 V). If the threshold of nMOS transistor which makes a cell transistor in case source potential is VB0 is set to Vth0 and the back-bias effect is set to deltaVth (> 0), Vthc can be expressed as shown in several 1, and VWL0 can be expressed as shown in several 2.
[0025]
[Equation 1]

$$Vthc = Vth0 + \Delta Vth$$

[0026]
[Equation 2]

$$VWL0 = VB1 + Vth0 + \Delta Vth$$

[0027] Here, when [approximate back-bias effect deltaVth of the threshold voltage Vth by primary formula of a source voltage, and] deltaVth=K*VB1, VWL0 comes to be shown in several 3. However, K is a back-bias dependence coefficient.
[0028]
[Equation 3]

$$VWL0 = VB1 + Vth0 + K * VB1$$

[0029] Moreover, when it is the supply voltage VCC to which the voltage of a storage node in case "1" data is memorized by the storage node of a cell is supplied by the device (i.e., if VC1=VB1=VCC), VWL0 comes to be shown in several 4.
[0030]
[Equation 4]

$$VWL0 = VCC + Vth0 + K * VCC$$

[0031] This VWL0 is the voltage level of an indispensable word line, and value deltaVWL=VWL-VWL0 which lengthened VWL0 serves as the operating voltage margin of a word line from the voltage level VWL of an actual word line.
[0032] Although it is made to generate by the pressure-up voltage occurrence circuit in a chip, when the voltage level of a word line usually sets the voltage level VWL of an actual word line to R*VCC here, operating voltage margin deltaVWL of a word line comes to be shown in several 5. However, R is a value between 1-2.
[0033]
[Equation 5]

$$\Delta VWL = R * VCC - (VCC + Vth0 + K * VCC)$$

$$= (R - 1 - K) * VCC - Vth0$$

[0034]
[Problem(s) to be Solved by the Invention] Although the motion which lowers supply voltage VCC to dynamic memory for low-power-izing was active in recent years, when supply voltage VCC was made low, there was a trouble where operating voltage margin deltaVWL of a word line will become small so that clearly from several 5.
[0035] If it considers data-hold time here although operating voltage margin deltaVWL of a word line can be extended in making low the threshold Vth0 of a cell transistor in case a source voltage is VB0, a threshold Vth0 cannot be made not much low.
[0036] that is, although drawing 7 shows the voltage Vgs pair drain current Ids property between the gate sources of nMOS transistor, if the voltage between the gate sources Vgs becomes below the threshold Vth, the drain current Ids will decrease exponentially with the inclination of about 1 law, and the drain current Ids at the time of voltage Vgs=0V between the gate sources will serve as Ids=I0xexp (-Vth/S)
[0037] However, I0 is the variation of the voltage between the gate sources Vgs required for the drain currents Ids and S at the time of voltage Vgs=Vth between the gate sources to change 1 figure of the drain currents Ids, and a unit is [mV/decade].

[0038] Here, simply, although the voltage Vgs pair drain current Ids property between the gate sources of nMOS will come to be shown in a dashed line 36 from the status shown as a solid line 35 and the drain current Ids in voltage Vgs=0 between the gate sources will increase as shown in drawing 7 if the threshold voltage Vth is reduced, this serves as the leakage current from the storage node of a cell, and data-hold time will become unable to satisfy a specification value.
[0039] Thus, when it does in this way although operating voltage margin deltaVWL of a word line can be extended in making low the threshold Vth0 of a cell transistor in case a source voltage is VB0, there is un-arranging [that data-hold time will become unable to satisfy a specification value].
[0040] In view of such a point, this invention can extend the operating voltage margin of a word line, moreover, enables it to secure a specification value as data-hold time, and aims at offering the dynamic memory which enabled it to correspond to low-battery-ization.
[0041]
[Means for Solving the Problem] In the dynamic memory to which the dynamic memory by this invention comes to have the memory cell which has a capacitor for a charge store, and an n channel insulated-gate type field-effect transistor for a charge transfer, the gate electrode of the n channel insulated-gate type field-effect transistor for a charge transfer constitutes a P type polysilicon contest layer, and the gate electrode of the n channel insulated-gate type field-effect transistor of the circumference circuit which controls an operation of a memory cell is constituted from an N type polysilicon contest layer.
[0042] Thus, when it constitutes the gate electrode of the n channel insulated-gate type field-effect transistor for a charge transfer from a P type polysilicon contest layer, even if it lowers the P type impurity concentration on the front face of a substrate of the gate electrode lower part of the n channel insulated-gate type field-effect transistor for a charge transfer and it makes a back-bias dependence coefficient small, the conventional threshold voltage can be secured as a threshold voltage in the case of memorizing "0" data.
[0043]
[Embodiments of the Invention] Drawing 1 is a rough cross section showing the important section of an example of the gestalt of operation of this invention, and the field oxide film to which 38 makes a P type substrate and 39 makes an isolation field, nMOS transistor to which 40 makes a cell transistor, and 41 are nMOS transistors of a circumference circuit.
[0044] Moreover, in the nMOS transistor 40 which makes a cell transistor, the source with which 42 consists of an N type diffusion layer, the drain with which 43 consists of an N type diffusion layer, the gate insulator layer which 44 becomes from a silicon oxide, and 45 are gate electrodes which consist of a P type polysilicon contest layer which comes to pour in a P type impurity.
[0045] Moreover, in the nMOS transistor 41 of a circumference circuit, the source with which 46 consists of an N type diffusion layer, the drain with which 47 consists of an N type diffusion layer, the gate insulator layer which 48 becomes from a silicon oxide, and 49 are gate electrodes which consist of an N type polysilicon contest layer which comes to pour in an N type impurity.
[0046] Namely, an example of the gestalt of operation of this invention constitutes the gate electrode of nMOS transistor of a circumference circuit from an N type polysilicon contest layer, and it constitutes like [others] the conventional dynamic memory shown in drawing 4 while it constitutes the gate electrode of nMOS transistor which makes a cell transistor from a P type polysilicon contest layer.
[0047] As the nMOS transistor 40 which makes a cell transistor here, and the nMOS transistor 41 of a circumference circuit are shown in drawing 2 , they can be created. In addition, 51 show the memory cell field among drawing 2 , and 52 shows the circumference circuit field.
[0048] That is, first, as shown in drawing 2 A, the silicon nitrides 53 and 54 are formed in the field (active region) which forms a transistor on a substrate 38.
[0049] Next, in order to form the field oxide film 39, then to control the threshold voltage Vth to carry out the selective oxidation of the non-active region, and to be shown in drawing 2B for isolation, the ion implantation of boron B is performed.
[0050] In this case, the ion implantation of boron B to the memory cell field 51 and the ion implantation of boron B of the circumference circuit field 52 are performed separately, and it may be made to change the concentration of boron B of the memory cell field 51, and the concentration of boron B of the circumference circuit field 52.
[0051] Next, as shown in drawing 2 C, the silicon oxide 55 used as a gate insulator layer is formed, and the polysilicon contest layer 56 used as a gate electrode is further formed on a silicon oxide 55.
[0052] Next, as similarly shown in drawing 2 C, a resist 57 is formed on the polysilicon contest layer of the circumference circuit field 52, and the ion implantation of boron B is performed in the polysilicon contest layer of the memory cell field 51.
[0053] Next, as shown in drawing 2 D, a resist 58 is formed on the polysilicon contest layer of the memory cell field 51, and the ion implantation of Lynn P or the arsenic As is performed in the polysilicon contest layer of the circumference circuit field 52.
[0054] In addition, the ion implantation of boron B to the polysilicon contest layer of the memory cell field 51 and the ion implantation of Lynn P to the polysilicon contest layer of the circumference circuit field 52 or the arsenic As may make sequence reverse.
[0055] Next, as shown in drawing 2 E, patterning of the gate electrode 45 of the nMOS transistor 40 which makes a cell transistor, and the gate electrode 49 of the nMOS transistor 41 of a circumference circuit is carried out.
[0056] Next, the ion implantation of Lynn P or the arsenic As can be performed, and as shown in drawing 1 , the nMOS transistor 40 which makes a cell transistor, and the nMOS transistor 41 of a circumference circuit can be created by forming the sources 42 and 46 and the drains 43 and 47.

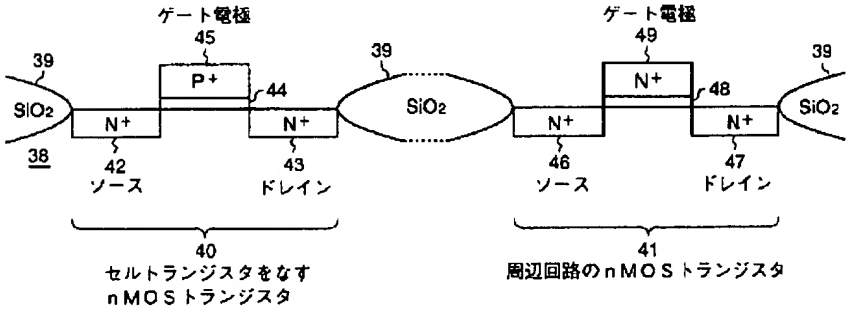
[0057] Drawing 3 shows the threshold voltage Vth pair source and the voltage Vsb property between substrates of nMOS transistor which makes a cell transistor here, and the threshold voltage Vth of nMOS transistor which makes a cell transistor can be expressed by Vth=Vfb+A.
[0058] However, Vfbs are the voltage decided by the work function difference of a gate electrode material and the substrate material under a gate electrode, and the so-called flat band voltage, and A is a constant decided by P type impurity concentration on the front face of a substrate under a gate electrode.
[0059] Here, the direction are formed in a P type polysilicon contest layer becomes high rather than flat band voltage's Vfb forming a gate electrode in an N type polysilicon contest layer.
[0060] Moreover, constant A becomes so large that the P type impurity concentration on the front face of a substrate under a gate electrode is high, and back-bias dependence coefficient K also has the correlation that the P type impurity concentration on the front face of a substrate becomes so large that it is high.
[0061] In addition, when the amount of ion implantation of the same P type impurity of type as the substrate front face under a gate electrode is made [many] to a gate electrode, there is the same effect as making high P type impurity concentration on the front face of a substrate under a gate electrode about the threshold voltage Vth.
[0062] Then, in forming the gate electrode of nMOS transistor which makes a cell transistor in a P type polysilicon contest layer, flat band voltage Vfb becomes large, and as the arrow head P1 shows to drawing 3 , it shifts the threshold voltage Vth pair source and the voltage Vsb property between substrates from the status shown as a solid line 60 in the status shown with the two-dot chain line 61, i.e., the orientation where a threshold Vth becomes high.
[0063] However, although back-bias dependence coefficient K can be made small by one side when reducing the amount of ion implantation of boron B to an active region, it can carry out to the status shown with a dashed line 62, i.e., the status take the threshold voltage which can secure a specification value as data-hold time, in this case from the status which shows the threshold voltage Vth pair source and the voltage Vsb property between substrates in drawing 3 with the two-dot chain line 61 as the arrow head P2 shows.
[0064] That is, when forming the gate electrode of nMOS transistor which reduces the amount of ion implantation of boron B to the field which forms nMOS transistor which makes a cell transistor, and makes a cell transistor in a P type polysilicon contest layer, as data-hold time, the threshold voltage which can secure a specification value can be maintained and back-bias dependence coefficient K can be made small.
[0065] Even if it reduces the amount of ion implantation of boron B to the field which forms the nMOS transistor 40 which makes a cell transistor here since the gate electrode 45 of the nMOS transistor 40 which makes a cell transistor is constituted from a P type polysilicon contest layer in an example of the gestalt of operation of this invention and it makes back-bias dependence coefficient K small, the conventional threshold voltage Vth0 is securable as a threshold voltage Vth0.
[0066] If it puts in another way, since the gate electrode 45 of the nMOS transistor 40 which makes a cell transistor is constituted from a P type polysilicon contest layer, it can reduce in the amount which can secure the conventional threshold voltage Vth0 for the amount of ion implantation of boron B to the field which forms the nMOS transistor 40 which makes a cell transistor as a threshold voltage Vth0, and back-bias dependence coefficient K can be made small.
[0067] Therefore, since according to an example of the gestalt of operation of this invention the operating voltage margin of a word line can be extended and a specification value can moreover be secured as data-hold time, it can correspond to low-battery-ization.
[0068] Moreover, in an example of the gestalt of operation of this invention, since [the gate electrode 49 of the nMOS transistor 41 of a circumference circuit] Lynn P.or the arsenic As which is an N type impurity is constituted from a polysilicon contest layer which comes to carry out an ion implantation, it does not lower the working speed of the nMOS transistor 41 of a circumference circuit.
[0069] In addition, although the case where the gate electrode 45 of the nMOS transistor 40 which makes a cell transistor, and the gate electrode 49 of the nMOS transistor 41 of a circumference circuit were constituted from a P type polysilicon contest layer in an example of the gestalt of operation of this invention was explained It can also consider as the polycide structure where the silicide compound which becomes the upper part of a P type polysilicon contest layer from tungsten W and silicon Si, or the silicide compound which consists of titanium Ti and silicon Si comes to deposit these gates electrode.
[0070]
[Effect of the Invention] As mentioned above, by having presupposed that the gate electrode of the n channel insulated-gate type field-effect transistor for a charge transfer is constituted from a P type polysilicon contest layer according to this invention Even if it lowers the P type impurity concentration on the front face of a substrate of the gate electrode lower part of the n channel insulated-gate type field-effect transistor for a charge transfer and it makes a back-bias dependence coefficient small Since the conventional threshold voltage is securable as a threshold voltage in the case of memorizing "0" data, the operating voltage margin of a word line can be extended, and moreover, as data-hold time, a specification value can be secured and it can correspond to low-battery-ization.

[Translation done.]

DRAWINGS

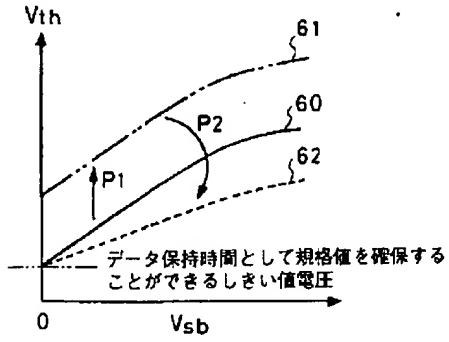
[Drawing 1]

本発明の実施の形態の一例の要部を示す概略的断面図



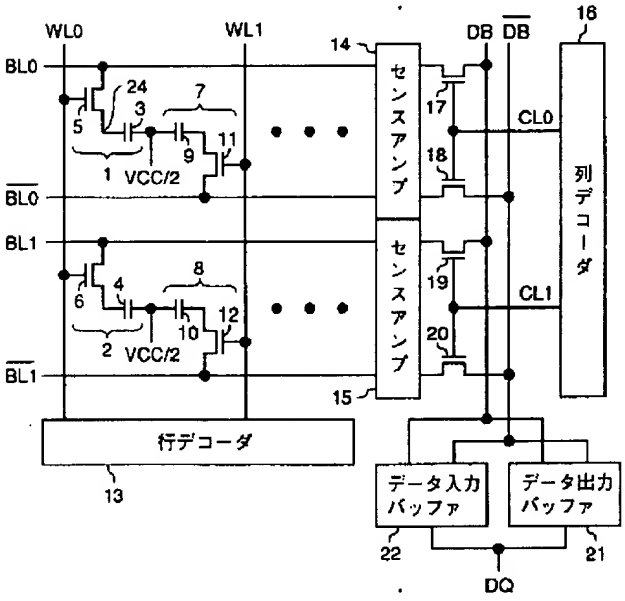
[Drawing 3]

セルトランジスタをなすnMOSトランジスタの
Vth－Vsb特性を示す図



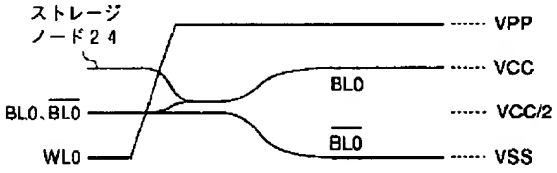
[Drawing 4]

ダイナミックメモリの一例の要部を示す回路図



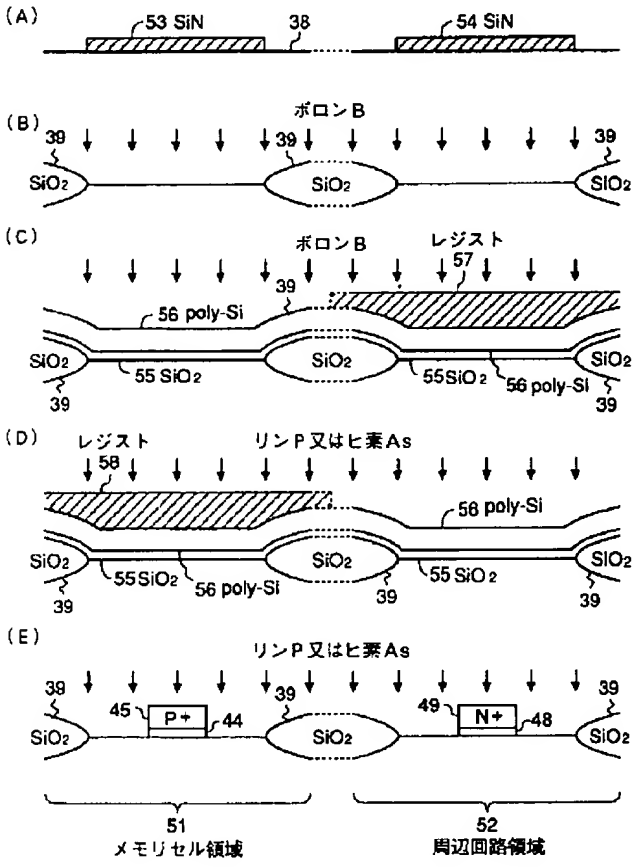
[Drawing 5]

図4に示すダイナミックメモリの読出し動作及び再書込み動作を示す概略的電圧波形図



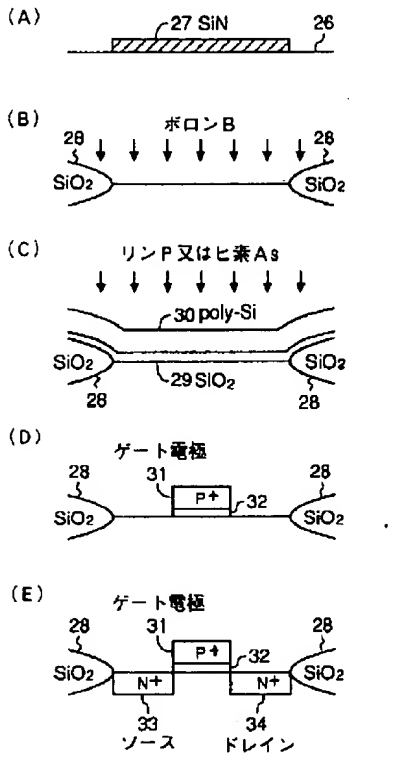
[Drawing 2]

セルトランジスタをなすｎＭＯＳトランジスタ及び周辺回路のｎＭＯＳトランジスタの作成過程を示す概略的断面図

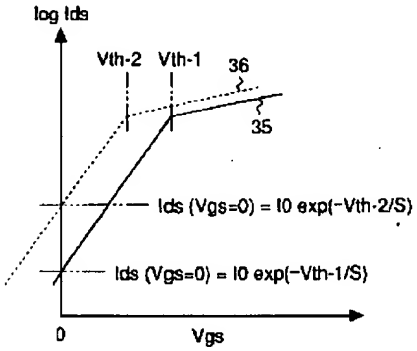


[Drawing 6]

nＭＯＳトランジスタからなるセルトランジスタの作成過程を示す概略的断面図



[Drawing 7]
nＭＯＳトランジスタのVgs－Ids特性を示す図



[Translation done.]